Preliminary Data Sheet
May 1992

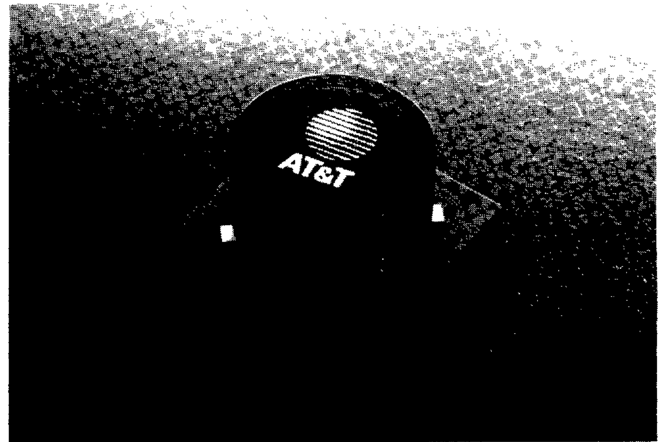
BEST-1 Series High-Performance ECL Gate Arrays

Features

- 1,000 and 4,000 equivalent logic gates
- Four programmable speed/power levels (unloaded, 2-input OR/NOR gates):
  — 700 ps @ 0.25 mW
  — 350 ps @ 0.5 mW
  — 250 ps @ 1.0 mW
  — 200 ps @ 2.0 mW
- Three levels of series gating (stacked logic)
- Three metal levels, including two mask-programmable levels
- 10KH or 100K ECL and TTL logic family interface
- Large function library
- Frequency response:
  — 2.0 GHz toggle frequency
  — 1.0 GHz ECL output buffer
  — 2.0 GHz ECL input buffer
- *Mentor Graphics** and Cadence Design Systems CAD support
- Operating junction temperature ranges from 0 °C to 125 °C for three levels of series gating and from –55 °C to +125 °C for two levels of series gating.

Description

The BEST-1 Series High-Performance ECL Gate Arrays use AT&T's bipolar-enhanced, super-self-aligned technology (BEST), which yields an f_T of 14 GHz at a highly manufacturable, minimum geometry of 1.5 µm. At modest power levels, BEST-1 gate arrays achieve operating frequencies greater than 1 GHz. The BEST-1 ECL gate array family combines advanced process technology with innovative design and high-performance packaging. Industry-standard CAD tools are integral to the design process.



* *Mentor Graphics* is a registered trademark of Mentor Graphics Corporation.

Table 1. BEST-1 Product Summary

Parameter	BE1000	BE4000
Equivalent Gates	1,048	4,196
Internal Cells	182	728
I/O Buffer Cells	48	108
Fixed Power and Ground Pads	32	38
Equivalent Gates (D flip-flop with clear)	728	2,912
Equivalent Gates (1-bit full adder)	1,001	4,004

Technology Overview

The BEST-1 family of gate-array standard cells is fabricated by using a nonoverlapping, super-self-aligned, bipolar process (see Figure 1). The process is oxide-isolated and uses 1.5 µm minimum drawn-feature-size (emitter strip width) design rules with a minimum transistor cell size of 280 µm². Three levels of metallization are used: two for interconnection wiring and the third for power-bus distribution.

The BEST-1 technology features NPN transistors with a typical f_T of 14 GHz and low parasitic capacitances. Polysilicon resistors with low parasitics and low temperature coefficients are also available. The emitter of the BEST-1 transistor is self-aligned to the base polysilicon electrode and separated from it by a 0.2 µm spacer. All polysilicon electrodes are silicided, which allows for small extrinsic base areas, very low base resistances, and an additional level of interconnect. Contacts are over the field-oxide for increased packing density and planarity. The polysilicon emitter serves as a diffusion source, which leads to shallow junctions and high f_T.

Table 2. Typical BEST-1 NPN Transistor Parameters

Parameter	Value	Unit
Emitter Dimensions	1.5 x 3	µm
Transistor Area	280	µm²
Gain (h_{FE})	100	—
Cut-off Frequency (f_T)	14	GHz
BV_{CEO}	7.5	V
BV_{CBO}	18	V
Emitter-base Capacitance	11	fF
Collector-base Capacitance	9	fF
Substrate Capacitance	29	fF
Base Resistance	625	Ω
Collector Resistance	150	Ω
Emitter Resistance	22	Ω
Early Voltage	30	V

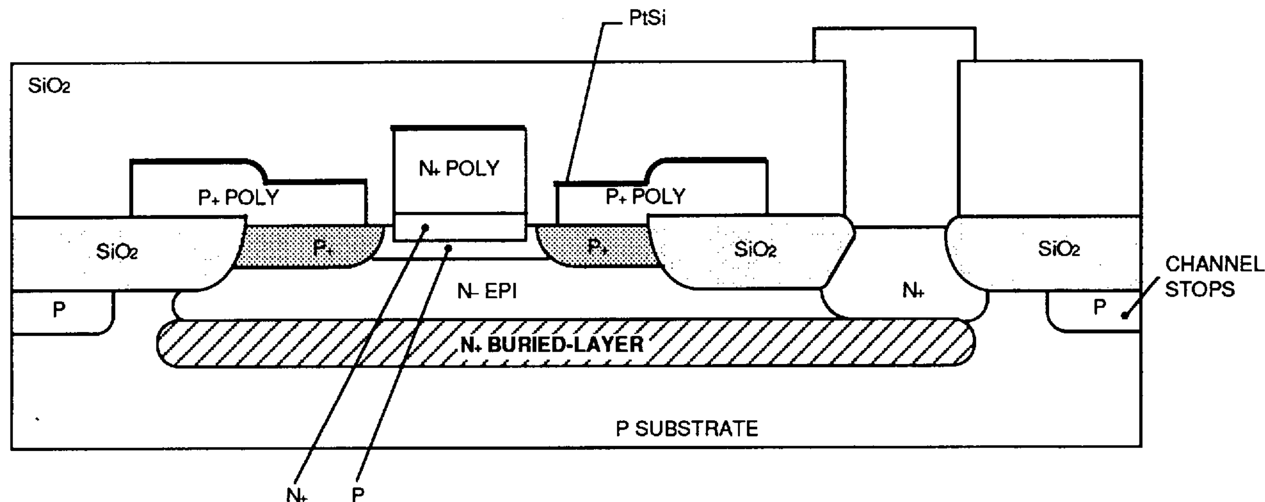


Figure 1. BEST-1 NPN Transistor Structure

AT&T Array Architecture

Overview

The BEST-1 Series of gate arrays consists of two products:

- BE1000 — 1,048 equivalent logic gates
- BE4000 — 4,196 equivalent logic gates

Layout

The BEI000 BEST-1 gate array features a highly efficient floor plan, optimized to use as much as 95% of the internal cells. As indicated in Figure 2, the BE1000 is rectangular with internal cells positioned in the center. Power supply pins, ground pins, and regulators are located at the corners. The perimeter is formed by eight groups of buffer cells and four separate grounds.

The 182 internal cells are arranged in seven rows, each containing 26 basic internal cells with a fixed height of 192 μm and width of 78 μm. At the right-hand end of each cell row is an internal regulator that provides the current source bias voltage and two reference voltages.

Two band gap references (BBG), one at the top left and another at bottom right, provide the ECL input threshold levels. Two other regulators (BREG), one at the top right and one lower left, provide internal reference levels to the I/O.

The BE1000 has a total of 48 I/O buffer cells which can be used as TTL or ECL input, output, or bidirectional pins.

The BE4000 gate array has a layout approach and features similar to the BE1000 gate array.

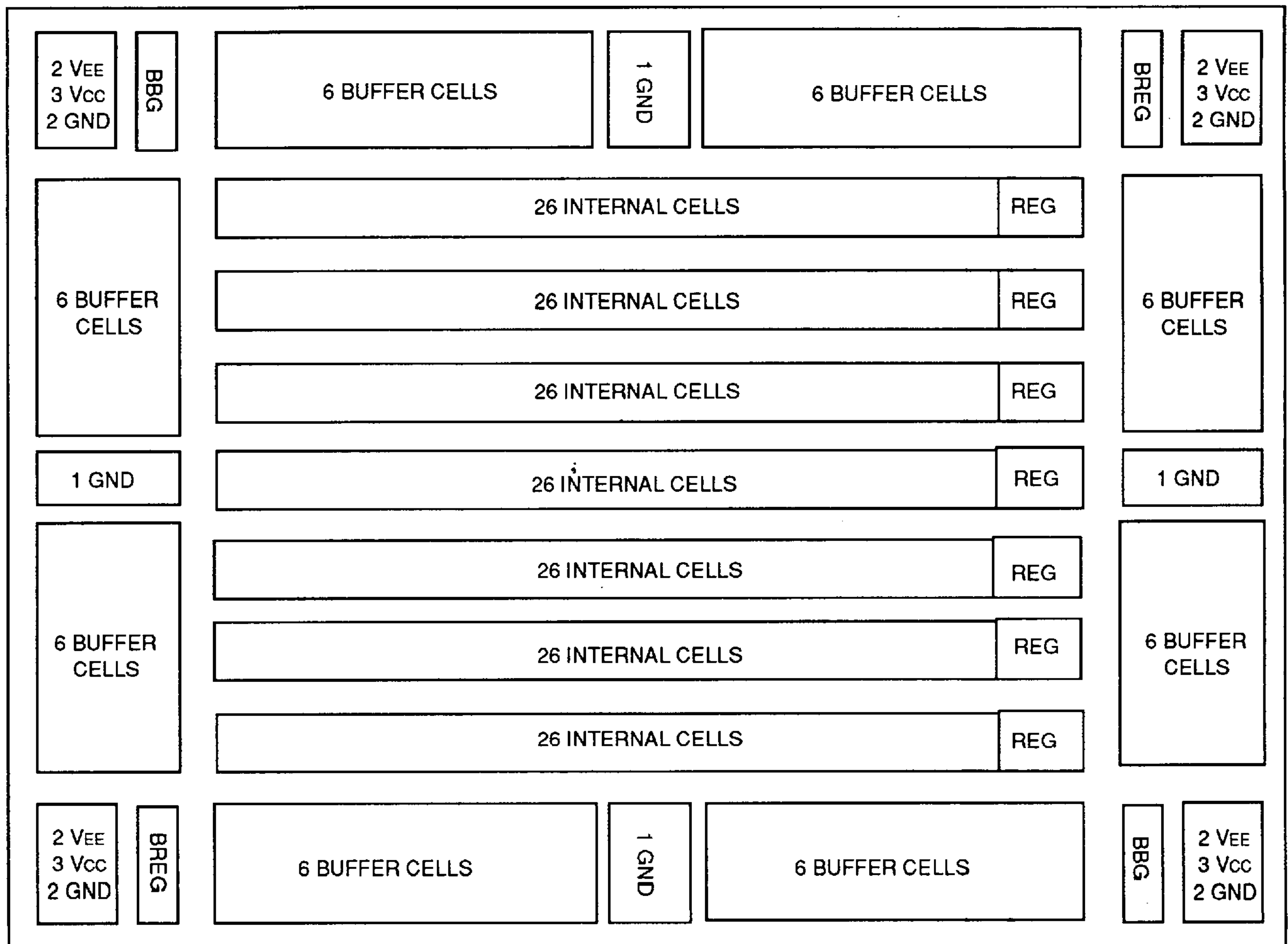


Figure 2. BE1000 Array Floor Plan

AT&T Array Architecture (continued)

Basic Internal Cell

The basic internal cell contains 22 NPN transistors and 29 polysilicon resistors. To minimize component count and power dissipation, functions are constructed from one or more cells by using up to three levels of series gating, and differential outputs are provided at two voltage levels (OX and OY). Figure 3 displays one example of a BEST-1 function block: a three-input, AND/NAND-gate schematic with three levels of series gating and programmable speed/power. Functions are programmed by changing the switch current source and the emitter-follower current source. Table 3 shows the four available power levels and their corresponding switch and emitter current sources.

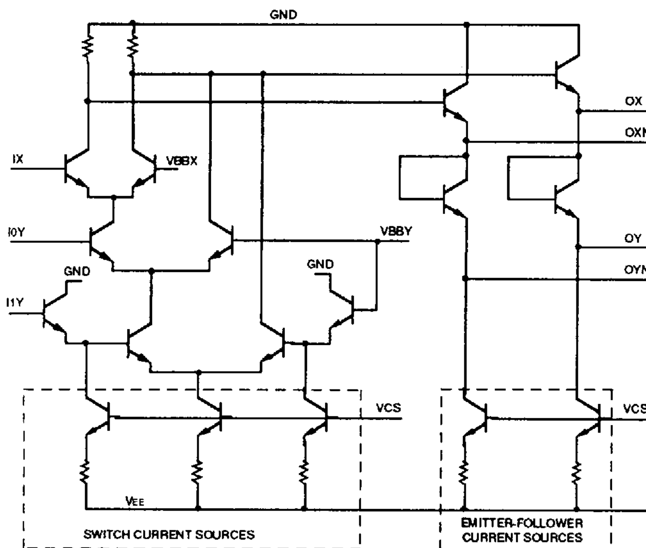


Figure 3. Three-Input, AND/NAND-Gate Schematic

Table 3. Functional Blocks

Power Levels	Switch Current Sources (µA)	Emitter-Follower Current Sources (µA)
Ultra-low	50	150
Low	100	300
Medium	200	550
High	400	1,000

The internal logic swing is typically 700 mV. Input and output signals are available at the top and bottom of the cell to improve routability, minimizing the number of feedthroughs required. Three levels of series gating permit the implementation of highly integrated logic functions. The levels of series gating for each function are listed in the Function-Block Library section. The operating junction temperature range of the BEST-1 gate arrays is –55 °C to +125 °C. Functions with three levels of series gating have a limited operating junction temperature range of 0 °C to 125 °C and supply voltage of –5.2 V, as shown in Table 4.

Table 4. Supply Voltage and Junction Temperature Operating Conditions

Series Gating Levels	Supply Voltage (V_{EE})	Junction Temperature Range
3	–5.2 V	0 °C to 125 °C
2	–5.2 V	–55 °C to +125 °C
2	–4.5 V	0 °C to 125 °C

I/O Buffer Cell

An I/O buffer cell contains 47 NPN transistors, four Schottky clamped transistors, four guard-ringed Schottky diodes, and 37 polysilicon resistors. These devices are used to construct a flexible I/O family, including 10KH and 100K ECL output buffers capable of driving 100 Ω and 50 Ω loads, and 3-state TTL output buffers. I/O cells are configurable independently to provide a universal range of input, output, and bidirectional interface options, as listed in Table 5.

Table 5. I/O Interfaces

Input	Output	Bidirectional
TTL	TTL Totem Pole TTL 3-state TTL Open Collector	TTL
10KH or 100K ECL Single Ended	10KH or 100K ECL Single Ended (50 Ω and 100 Ω loads)	10KH or 100K ECL Single Ended
10KH or 100K ECL Differential	10KH or 100K ECL Differential (50 Ω and 100 Ω loads)	—

BEST-1 Characteristics

The following information includes a summary of dc input and output characteristics for the I/O buffers contained in the BEST-1 function library.

TTL Characteristics

Table 6. Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Supply Voltage*	V_{CC}	0	6.5	V
Input Voltage	V_{IN}	0	5.5	V
Storage Temperature	T_{stg}	–65	150	°C

* A negative supply must be provided for ECL.

Table 7. Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Junction Temperature	T_J	–55†	—	125	°C
Input Voltage‡					
Low	V_{IL}	—	—	0.8	V
High	V_{IH}	2.0	—	—	V

* A negative supply must be provided for ECL.

† Only two levels of logic gating are permitted at junction temperatures less than 0 °C.

‡ Input voltages are guaranteed in a noise-free environment. In this case, the sum of the steady-state input, any noise signals on the input, and any noise on the power supply lead cannot exceed the guaranteed level.

Table 8. dc Characteristics* (V_{CC} = 5.0 ± 0.5 V)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Voltage						
High	V_{OH}	V_{CC} = min; I_{OH} = –1 mA	2.7	—	—	V
Low	V_{OL}	V_{CC} = min; I_{OL} = 24 mA	—	0.35	0.5	V
Output Voltage (low power)						
High	V_{OH}	V_{CC} = min; I_{OH} = –450 µA	2.7	—	—	V
Low	V_{OL}	V_{CC} = min; I_{OL} = 8 mA	—	0.35	0.5	V
Output Off Current						
High	I_{OZH}	V_{CC} = max; V_{OUT} = 5.5 V	—	—	50	µA
Low	I_{OZL}	V_{CC} = max; V_{OUT} = 0.4 V	—	—	–50	µA
Input Current						
High	I_{IH}	V_{CC} = max; V_{IN} = 5.5 V	—	—	100	µA
Low	I_{IL}	V_{CC} = max; V_{IN} = 0 V	—	—	–400	µA
Output Short-circuit Current	I_{OS}	V_{CC} = max; V_{OUT} = 0 V	–40	—	–225	mA
Output Short-circuit Current (low power)	I_{OS}	V_{CC} = max; V_{OUT} = 0 V	–35	—	–90	mA

* Data measured at thermal equilibrium.

BEST-1 Characteristics (continued)

ECL I/O Characteristics

Table 9. Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{EE}	0	–6.5	V
Input Voltage				
10KH	—	0	–5.7	V
100K	—	0	–4.8	V
Storage Temperature	T_{stg}	–65	150	°C

Table 10. Operating Conditions

Parameter	Symbol	Junction Temperature (T_J)	Min	Typ	Max	Unit
Supply Voltage						
100K	V_{EE}	0 °C to 125 °C*	–4.2	–4.5	–4.8	V
10KH	V_{EE}	–55 °C to +125 °C†	–4.7	–5.2	–5.7	V
Low Input Voltage (10KH)	V_{IL}	0 °C to 125 °C	—	—	–1.48	V
Low Input Voltage (100K)	V_{IL}	0 °C to 125 °C	—	—	–1.475	V
High Input Voltage (10KH)	V_{IH}	0 °C	–1.17	—	—	V
		25 °C	–1.13	—	—	V
		125 °C	–1.07	—	—	V
High Input Voltage (100K)	V_{IH}	0 °C to 125 °C	–1.165	—	—	V

* Function blocks with three levels of series gatings are not permitted for $V_{EE} = -4.5 \pm 0.3$ V operation.

† Function blocks with three levels of series gating are not permitted for $T_J < 0$ °C.

Note: 100K ECL levels are only guaranteed over a junction temperature range of 0 °C to 125 °C.

BEST-1 Characteristics (continued)

ECL I/O Characteristics (continued)

Table 11. dc Characteristics* (V_{EE} = –4.5 ± 0.3 V for 100K and –5.2 ± 0.5 V for 10KH)

Parameter	Symbol	Junction Temperature (T_J)	Min	Max	Unit
Output Low Voltage (low and medium power) (10KH)	V_{OL}	0 °C 25 °C 125 °C	–1.950 –1.950 –1.950	–1.650 –1.650 –1.620	V V V
Output Low Voltage (low and medium power) (100K)	V_{OL}	0 °C to 125 °C	–1.810	–1.620	V
Output High Voltage (low and medium power) (10KH)	V_{OH}	0 °C 25 °C 125 °C	–1.000 –0.960 –0.900	0.840 0.810 0.740	V V V
Output High Voltage (low and medium power) (100K)	V_{OH}	0 °C to 125 °C	–1.025	–0.880	V
Input Current (V_{IN} = –0.5 V) Standard Input Buffers Clock Input Buffers (ECI, ECN) Low-power, Balanced, Clock Input Buffer (EBCBL) Balanced Clock Input Buffer (EBCB)	I_{IH}	–55 °C to +125 °C	— — — —	8 16 80 160	µA µA µA µA

* Data measured at thermal equilibrium.

Note: Low-power buffers loaded 100 Ω to –2 V. Medium-power buffers loaded 50 Ω to –2 V.

Packaging

The BEST-1 Series of gate arrays is available in a variety of standard packages as shown in Table 12.

Table 12. Best-1 Gate Array Packages

Package Type	Number of Package Leads	Number of Signal Leads BE1000	Number of Signal Leads BE4000	Power Diss * (W)	Power Diss* (W) w/Heat Sink	Power/ Ground Planes	Her-metic
Plastic Leaded Chip Carrier (PLCC)†	44	32	—	1.25	1.5	No	No
	68	48	—	1.5	2.0	No	No
Ceramic Pin Grid Array (CPGA)	119	—	108	5	10	Yes	Yes
	163	—	108	6	12	Yes	Yes
Plastic Pin Grid Array (PPGA)	71	48	—	3.25	5.2	No	No

* Power dissipation assumes 400 fpm air flow and 70 °C ambient termperature and 125 °C junction temperature.

† PLCC packages are available in straight, gull-wing, or J-leaded pin configurations.

BEST-1 Gate Array Design Process

CAD Development System

AT&T offers two choices for the design of BEST-1 ECL gate arrays. Customers can use AT&T-supplied libraries and Cadence, *Mentor Graphics, Viewdraw**, or *Verilog-XL*† design software to complete the front-end design and then transmit a completed netlist to AT&T for layout. Or, AT&T can perform the entire front-end design for the customer on a turnkey basis.

In both cases, AT&T employs a powerful set of proprietary tools for back-end design. Back-end design includes automatic layout (placement and routing), design and electrical rules checking, resimulation using extracted layout parasitics, and photomask and test program generation.

AT&T carries an inventory of gate-array wafers, which have been processed up to the metallization steps. The metal layers are added as per the customer's option, and prototypes are fabricated and delivered. Figure 4 shows the various steps of the CAD design process.

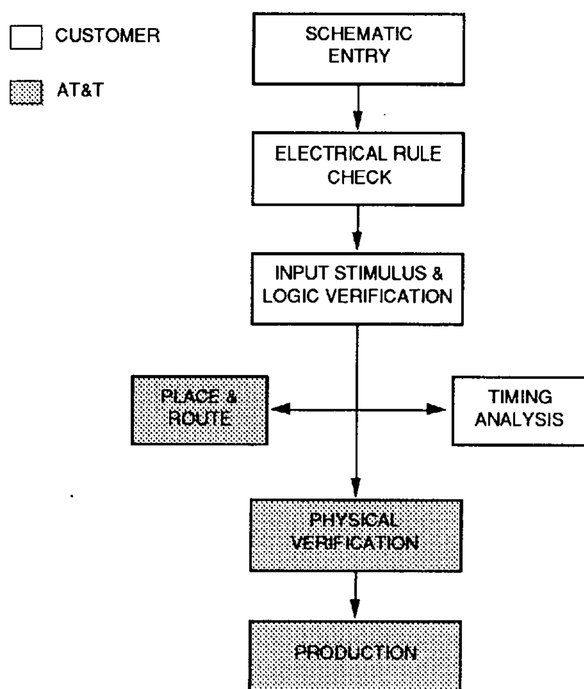


Figure 4. Best-1 Design Cycle

Software Requirements

- Cadence Design Systems, Inc.
  - — v4.2 Support
  - — Front-end Design Kit, Composer, Electrical Rule Check, *Verilog-XL, Verifault-XL*†, Delay Calculation
- Mentor Graphics Corporation
  - — v8.x Support
  - — Front-end Design Kit, Delay Calculation, *Design Architect*‡, Electrical Rule Check, *QuickSim* II‡, *QuickFault*‡, *QuickPath*‡
- *Viewdraw-> Verilog*-XL
  - — Schematic Entry, Electrical Rule Check, *Verilog*-XL, Delay Calculation

AT&T-Customer Responsibilities

- Information supplied by AT&T:
  - — All necessary libraries with symbol, functional, and timing information
  - — Design manual
- Information returned by the customer:
  - — Completed netlist (EDIF 2.00)
  - — Test vectors
  - — Pinout diagram
  - — Completed copy of AT&T's bipolar IC design specification document
- Service provided by AT&T:
  - — All necessary technical support and consultation
  - — Physical design layout
  - — Extraction of parasitics
  - — Back annotation to the customer's CAD system (if applicable)
  - — Manufacture

* *Viewdraw* is a registered trademark of Viewlogic Systems, Inc.
† *Verilog-XL* and *Verifault-XL* are registered trademarks of Cadence Design Systems, Inc.
‡ *QuickSim* II, *QuickFault, QuickPath,* and *Design Architect* are trademarks of Mentor Graphics Corporation.

Function-Block Library

The predefined function blocks in the BEST-1 library include inverters, gates, decoders, multiplexers, adders, flip-flops, and latches. Each function is programmable to any of the four speed/power levels. The currently available function blocks include:

- 37 combinational blocks
- 30 sequential blocks
- 40 ECL I/O buffers
- 30 TTL I/O buffers

These function blocks are common for both gate-array and standard-cell products. This provides the customer with the option of selecting either gate-array or standard-cell implementation at the time of front-end design completion. Also, gate arrays can be easily converted to standard cells to meet high-volume manufacturing requirements. For a more detailed description of the BEST-1 standard-cell design process, refer to the *BEST-1 Gate Array and Standard Cell Design Manual.*

Table 13. Combinational Logic

Cell	Function	Size (sites)	Series Gating
INV1	Buffer-Inverter	1	1
RCR1	Differential Buffer-Inverter	1	1
OR2	2-Input OR/NOR	1	1
OR4	4-Input OR/NOR	1	1
OR8	8-Input OR/NOR	2	1
OR12	12-Input OR/NOR	2	1
AND2	2-Input AND/NAND	1	2
AND3	3-Input AND/NAND	1	3
AND4	4-Input AND/NAND	2	3
XOR21	2-Input XOR/XNOR	1	2
XOR23	3-OR/2-XOR/XNOR	1	2
XOR27	7-OR/2-XOR/XNOR	2	2
XOR3	3-Input XOR/XNOR	2	3
XOR4	4-Input XOR/XNOR	2	3
MDX1E	1:2 Decoder with Enable	1	2
MDX2	2:4 Decoder	2	2
MDX2E	2:4 Decoder with Enable	2	3
MUX2	2:1 Multiplexer	1	2
MUX2E	2:1 Multiplexer with Enable	1	3
MUX4	4:1 Multiplexer	2	2
MUX4E	4:1 Multiplexer with Enable	2	3
OA2I1N	2-NOR/2-AND/NAND	1	2
OA2I2N	2-NOR/2-OR/2-AND/NAND	1	2
OA2N1N	2-OR/2-AND/NAND	1	2
OA2N2N	2-OR/2-OR/2-AND/NAND	1	2
OA3I1N	3-NOR/2-AND/NAND	1	2
OA3I2N	3-NOR/2-OR/2-AND/NAND	1	2
OA3I3N	3-NOR/3-OR/2-AND/NAND	1	2
OA3N1N	3-OR/2-AND/NAND	1	2
OA3N2N	3-OR/2-OR/2-AND/NAND	1	2
OA3N3N	3-OR/3-OR/2-AND/NAND	1	2
OA4I4N	4-NOR/4-OR/2-AND/NAND	2	2
OA4N4N	4-OR/4-OR/2-AND/NAND	2	2
ADD1	2-Bit Full Adder	2	2
AN1D1I	Differential AND/NAND	1	2
OR2D	Differential 2-Input OR/NOR	1	2
CKDR	Internal Clock Buffer	1	1

Function-Block Library (continued)

Table 14. Sequential Blocks

Cell	Function	Size (sites)	Series Gating
F1SA	D-Type Flip-Flop	2	2
F1SB	D-Type F/F with Preset	2	2
F1SC	D-Type F/F with Clear	2	2
F1DA	Differential D-Type F/F	2	2
F1DB	Differential D-Type F/F with Preset	2	2
F1DC	Differential D-Type F/F with Clear	2	2
F2SA	2:1 MUX Flip-Flop	2	3
F2SB	2:1 MUX F/F with Preset	2	3
F2SC	2:1 MUX F/F with Clear	2	3
F2DA	Differential 2:1 MUX F/F	2	3
F2DB	Differential 2:1 MUX F/F with Preset	2	3
F2DC	Differential 2:1 MUX F/F with Clear	2	3
F3SA	D-Type Latch	1	2
F3SB	D-Type Latch with Preset	1	2
F3SC	D-Type Latch with Clear	1	2
F3DA	Differential D-Type Latch	1	2
F3DB	Differential D-Type Latch with Preset	1	2
F3DC	Differential D-Type Latch	1	2
F4SA	2:1 MUX Latch	2	3
F4SB	2:1 MUX Latch with Preset	2	3
F4SC	2:1 MUX Latch with Clear	2	3
F4DA	Differential 2:1 MUX Latch	2	3
F4DB	Differential 2:1 MUX Latch with Preset	2	3
F4DC	Differential 2:1 MUX Latch with Clear	2	3
F5DA	Differential D-Type F/F	2	2
F5DB	Differential D-Type F/F with Preset	2	2
F5DC	Differential D-Type F/F with Clear	2	2
F7DA	Differential D-Type Latch	1	2
F7DB	Differential D-Type Latch with Preset	1	2
F7DC	Differential D-Type Latch with Clear	1	2

Table 15. ECL Input Buffers

Cell	Function	Size (sites)	Series Gating
E12N2	ECL Input Buffer	1	1
E12N2L	Low-Power ECL Input Buffer	1	1
EBI2	Balanced Input Buffer	2	1
EB12N2	Balanced Input Buffer	2	1
EBI2N2L	Low-Power Balanced Input	2	1
ECI	High-Fan-out Inverting Input	1	1
ECIL	Low-Power, High-Fan-out Inverting Input	1	1
ECN	High-Fan-out Input	1	1
ECNL	Low-Power, High-Fan-out Input	1	1
EBCB	High-Fan-out Balanced Input	2	1
EBCBL	Low-Power, High-Fan-out Balanced Input	2	1

Function-Block Library (continued)

Table 16. ECL 10KH Output Buffers

Cell	Function	Size (sites)	Series Gating
X2LI	Low-Power Inverting Output	1	1
X2LN	Low-Power Output	1	1
X2LB	Low-Power Balanced Output	2	1
XBLB	Low-Power Balanced Output	2	1
X2MI	High-Power Inverting Output	1	1
X2MN	High-Power Output	1	1
X2MB	High-Power Balanced Output	2	1
XBMB	High-Power Balanced Output	2	1

Table 17. Bidirectional ECL 10KH Buffers

Cell	Function	Size (sites)	Series Gating
IOELI	Low-Power Buffer	1	1
IOELN	Low-Power Buffer	1	1
IOEMI	High-Power Buffer	1	1
IOEMN	High-Power Buffer	1	1

Table 18. ECL 100K Output Buffers

Cell	Function	Size (sites)	Series Gating
X2LIK	Low-Power Inverting Output	1	1
X2LNK	Low-Power Output	1	1
X2LBK	Low-Power Balanced Output	2	1
XBLBK	Low-Power Balanced Output	2	1
X2MIK	High-Power Inverting Output	1	1
X2MNK	High-Power Output	1	1
X2MBK	High-Power Balanced Output	2	1
XBMBK	High-Power Balanced Output	2	1

Table 19. Bidirectional ECL 100K Buffers

Cell	Function	Size (sites)	Series Gating
IOELIK	Low-Power Buffer	1	1
IOELNK	Low-Power Buffer	1	1
IOEMIK	High-Power Buffer	1	1
IOEMNK	High-Power Buffer	1	1

Function-Block Library (continued)

Table 20. Special Buffers

Cell	Function	Size (sites)	Series Gating
ECIDR	High-Fan-out Inverting Buffer	1	1
ECIDRL	Low-Power, High-Fan-out Inverting Buffer	1	1
ECNDR	High-Fan-out Buffer	1	1
ECNDRL	Low-Power, High-Fan-out Buffer	1	1
TSI2	Inverting 3-State Control Buffer	1	1
TSN2	3-State Control Buffer	1	1
XVBB	ECL Threshold Reference	1	1

Table 21. TTL Input Buffers

Cell	Function	Size (sites)	Series Gating
TI2N2	TTL Input Buffer	1	1
TI2N2L	Low-Power TTL Input	1	1
TI2	Low-Power Inverting TTL Input	1	1
TN2	Low-Power TTL Input	1	1
TCI	High-Fan-out Inverting Input	1	1
TCIL	Low-Power, High-Fan-out Inverting Input	1	1
TCN	High-Fan-out Input	1	1
TCNL	Low-Power, High-Fan-out Input	1	1
TSI1	Inverting 3-State Control Buffer	1	1
TSN1	3-State Control Buffer	1	1

Function-Block Library (continued)

Table 22. TTL Output Buffers

Cell	Function	Size (sites)	Series Gating
X2IO	Inverting Open Collector	1	1
X2IOL	Low-Power Inverting Open Collector	1	1
X2IT	Inverting Totem Pole	1	1
X2ITL	Low-Power Inverting Totem Pole	1	1
X2IZ	Inverting 3-State	1	1
X2IZL	Low-Power Inverting 2-State	1	1
X2NO	Open Collector	1	1
X2NOL	Low-Power Open Collector	1	1
X2NT	Totem Pole	1	1
X2NTL	Low-Power Totem Pole	1	1
X2NZ	3-State	1	1
X2NZL	Low-Power 3-State	1	1
XLIT	Low-Power Inverting Totem Pole	1	1
XHIT	Low-Power Inverting Totem Pole	1	1

Table 23. TTL Bidirectional Buffers

Cell	Function	Size (sites)	Series Gating
IOTIZ	Bidirectional Buffer	1	1
IOTIZL	Low-Power Bidirectional	1	1
IOTNZ	Bidirectional Buffer	1	1
IOTNZL	Low-Power Bidirectional	1	1

Quality and Reliability

Quality

AT&T's manufacturing quality starts with purchased material quality. The purchase orders and their associated drawings include inspection information used to verify the quality of incoming materials at the factory receiving dock.

Each shop operation is covered by instructions and specifications contained in controlled documents. Manufacturing processes are monitored on-line by using statistical-process-control tools. Maintenance and calibration of production and test equipment are performed regularly.

Electrical parameter tests, predicated on a sampling basis, are performed immediately prior to shipment. The acceptance tests further ensure that device specifications and quality levels are being met. Failure-mode analysis (FMA) is used throughout the manufacturing process to identify those mechanisms responsible for device failure.

Periodic audits are conducted by Quality Assurance personnel to verify that all parts of the quality program are in place and being maintained.

Reliability

After qualification and during production, tests are conducted in a two-level monitoring program to ensure continued high reliability. In one level, tests are conducted for extended life and simulate a 25-year product life. Tests at this level are conducted every quarter. Tests in the other level simulate a nine-year product life and are conducted monthly. The sampling programs, stress conditions, and stressing times are selected to ensure that reliability goals are being met.

The reliability monitoring program consists of three tests. The first test, high-temperature operating bias/high-temperature high bias (HTOB/HTHB), accelerates failure mechanisms sensitive to high-temperature and voltage stresses. The failure mechanisms may be chip-oriented: for example, ionic drift, electrothermal migration, oxide breakdown, or silicon material defects. HTOB/HTHB stress conditions for the extended-life test are 125 °C for 3,000 hours to 150 °C for 525 hours. The monthly monitor stress conditions are 125 °C for 1,000 hours.

The second test, a package test, is temperature/humidity bias (THB), which checks the chip-to-package interface. High humidity in the presence of electrical bias promotes electrochemical corrosion, electrothermal migration, and other chemical reactions involving the presence of water. THB tests are conducted at 85 °C and 85% RH. The extended-life test is performed for 1,000 hours, while the monthly monitor is conducted for 240 hours.

The third test, temperature cycling (TC), applies thermally induced stress to ICs to accelerate material fatigue and precipitate failures associated with thermal-expansion mismatches. The TC test stresses ICs from –65 °C to +150 °C without bias. The extended-life stress duration is 300 cycles, while the monthly monitor duration is 100 cycles.

Detailed information regarding the quality and reliability program can be obtained from the *AT&T Quality and Reliability Manual.*

Electrostatic Discharge (ESD) Testing

AT&T employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. BEST-1 gate arrays meet Class 2 (greater than 500 V) HBM ESD protection for all input, output, and bidirectional leads.